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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant :	Keith Dow	Art Unit :	2112
Serial No.:	09/461,643	Examiner :	Christopher E. Lee
Filed :	December 14, 1999	Assignee :	Intel Corporation

Title : IMPROVED SIGNAL ROUTING BETWEEN A MEMORY CONTROL UNIT AND A MEMORY DEVICE

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY BRIEF

Pursuant to 37 C.F.R. § 1.193(b)(1), Applicant responds to the new points raised in the Examiner's Answer dated April 4, 2004, as follows.

At page 3, line 20: The Examiner's Answer contends that the Applicant Admitted Prior Art (hereinafter "AAPA") teaches first and second signal lines formed on the same first layer of a circuit board.

Applicant respectfully submits that no such "teaching" is found in the AAPA. Rather, Applicant respectfully submits that, as a result of congestion in the vicinity of pins on the memory unit, the AAPA signal lines into and out of the memory unit often must be formed on different layers of a circuit board.

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Further, rather than accept this state of the art, Applicant has developed systems and techniques that wherein first and second signal lines can each be formed on the same first layer of a circuit board. This limitation appears in the independent claims and further distinguishes the claims from the AAPA.

At page 4, line 19 - page 5, line 4 and page 17, line 12 - page 18, line 6: The Examiner's Answer contends that U.S. Patent No. 6,160,716 to Perino et al. (hereinafter "Perino") does not teach away from a non-grounded gap but rather teaches one of ordinary skill to choose whether or not to place a ground gap between signal lines based on various factors. These factors include the possibility of having a large spacing between traces and the desirability of minimizing interference between traces.

As cited in the Appeal Brief, Perino expressly teaches away from signal lines being separated by a non-grounded gap, and hence teaches away from the claims. Although Perino's figures show non-grounded gaps, Perino's text is quite clear and persistent in his disparagement of such gaps.

This said, Applicant does agree with the Examiner that the decision regarding whether or not to place a ground gap between signal lines is design choice generally made in consideration of various factors, including those cited. However, these factors clearly militate in favor of the non-obviousness of the claims. In particular, since the claimed first and second traces are connected to the same first pin, a large spacing between the first and second traces cannot be maintained. As claimed, at some point, the first and second traces must approach one another at the first pin. Since the first and second traces

must approach one another at the first pin, one of ordinary skill would feel that intervening ground traces are more desirable, rather than less desirable, since there is no possibility of maintaining a large spacing between traces.

This understanding is illustrated by the AAPA itself. Attention is respectfully directed to FIG. 2 which shows a ground trace (i.e., ground trace 165) separating signal lines when they are connected to the same first pin. The illustrated ground trace contributes to the congestion in the vicinity of the pin, as discussed at page 2, line 12 of the specification. The ground trace is hence undesirable on this ground. Nevertheless, the AAPA shows such a ground trace. Thus, the contention of page 5, lines 1-4 (i.e., that since the AAPA's signal lines are "one single connection line," one of ordinary skill would not place a ground trace between such signal lines) ignores the express, contrary teachings of the AAPA and amounts to a false conclusion and one which is unsupported by the record. Instead, the AAPA itself teaches that it is desirable to locate a ground trace between the first and second traces in the vicinity of the same pin, even when the first and second traces connect to the same pin and when the vicinity of the pin is congested.

Since one of ordinary skill who followed the Examiner's contentions would conclude that decreased spacing between signal lines results in increased need for a ground trace separating such lines, and since the AAPA shows such a ground trace in the face of undesirable congestion, Applicant respectfully reiterates that any rejection over this art cannot be sustained.

At page 6, line 1 - 7, page 9, line 3-9, and page 11, line 14-20: The Examiner's Answer contends that Applicant's recitation of a specific separation distance is not patentably significant.

In light of the Examiner's arguments discussed immediately above, Applicant respectfully disagrees. In particular, it is respectfully submitted that this contention is logically inconsistent with the impact of trace spacing on the desirability of ground traces. If a decision regarding the placement of a ground gap between signal lines is based, at least in part, on the ability to have a large spacing between signal lines, it is respectfully submitted that the claimed separation distance is relevant to the patentability of the claims.

At page 15, line 11 - 15: The Examiner's Answer appears to contend that, in light of the AAPA teaching of signal lines connected to the same pin, Perino's teaching away from connected signal lines is irrelevant.

Applicant respectfully disagrees. "As a 'useful general rule,' … references that teach away cannot serve to create a prima facie case of obviousness." *McGinley v. Franklin Sports*, Inc., 262 F.3d 1339, 1354 (Fed. Cir. 2001) (citing *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994)). Applicant is not contending that signal lines connected to the same pin are not described or suggested by the AAPA, but rather Applicant contends that any combination involving Perino is improper in light of Perino's express teachings away from signal lines connected to the same pin.

Applicant also wishes to point out that neither the Examiner's Answer nor any paper of record suggests any basis for ignoring this general rule and maintaining the obviousness rejection over Perino.

At page 16, line 1 - 8: In contrasting Example B of FIG. 8 with Example A of FIG. 8, the Examiner's Answer essentially contends that Example B operates by an unknown but somehow distinct physical mechanism to achieve the "same asserted advantage" of eliminating reflected signals and signal deterioration caused by mismatched impedance. Applicant disputes this conclusion as false and further contends that it is unsupported by Perino or any other art of record.

As discussed in the Appeal Brief, Perino describes that reflected signals and mismatched impedance are eliminated by maximizing the width of traces to reduce the impedance of those traces. Thus, Perino only provides a rationale for maximizing the width of signal lines, rather than achieving the proposed combination of Perino with the AAPA.

The Examiner's Answer contends that these express teachings regarding the maximization of the width of traces are somehow applicable only to Example A and not to Example B of FIG. 8. Applicant respectfully disagrees. Rather, Applicant respectfully submits that the physical laws governing the operation of Example A also govern the operation of Example B and thus the approach of maximizing line width to reduce impedance mismatch is applicable to both. This conclusion is supported by Perino himself. Attention is respectfully directed to col. 5, line 41 where the impedance of the 8 mil traces of Example B of FIG. 8 is denoted as 55 ohms, whereas the impedance

of the 12.5 mil trace of Example A of FIG. 8 is denoted as 45 ohms at col. 5, line 29. The impedance of Example B is clearly higher than the impedance of Example A. As such, the increased impedance of Example B does not match low impedance lines as closely, nor eliminate reflected signals and signal deterioration to the same extent. See, e.g., col. 5, line 30-33 and col. 2, line 15-33 of Perino.

Further, even if Example B somehow exploited unknown and undescribed physical mechanisms to escape the laws of nature, failure to consider the express teachings of Perino is still improper. "[A] prior patent must be considered in its entirety, i.e., as a whole, including portions that would lead away from the invention in suit." *W.L. Gore & Associates, Inc. v. Garlock*, Inc., 721 F.2d 1540, 1550, (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984) (emphasis added). Since Perino expressly teaches that increased impedance increases reflected signals and signal deterioration, any conclusion to the contrary is improper absent any support in the art of record.

Since Perino only provides a rationale for maximizing the width of signal lines, Applicant respectfully submits that there is no suggestion to combine relevant to the proposed combination of Perino with the AAPA and that a *prima facie* case of obviousness has not been established.

At page 19, line 18 - 19: The Examiner's Answer contends that "the method steps of claim 8 are performed by means for function."

Applicant respectfully disagrees. A claim element deserves means-plus-function treatment when "expressed as a means ... for performing a specified function without the recital of structure

[or] material ... in support thereof." O.I. Corp. v. Tekmar Co. Inc., 115 F.3d 1576, 1583 (Fed. Cir. 1997). Since the method of claim 8 does not express any element as a means for performing a specified function, none of the recited elements deserve means-plus-function treatment.

At page 20, line 20 - 21: The Examiner's Answer contends that "the method steps of claim 14 should have been performed by a means for manufacturing."

Applicant respectfully disagrees. Rather, Applicant submits that the method recited in claim 14 is independent of any means for manufacturing.

For these reasons, and the reasons stated in the Appeal Brief, Applicant submits that the final rejection should be reversed.

No fee is believed to be due. Please apply any charges not covered or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: June 30, 2004

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